

TA 5.5: A 160,000 Transistor GaAs Microprocessor

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A single-chip GaAs microprocessor includes a Ling-adder-based ALU, 32b shifter, 32-word register file, 4-word write buffer, 32-word on-chip instruction cache, support for 2 levels of off-chip instruction and data caches and an asynchronous system interface. It is in direct-coupled FET logic (DCFL) and integrates 160,000 transistors on a 13.9x7.8mm² die. When operating from a 2V supply, the chip typically dissipates 24W. A micrograph of the integrated circuit is shown in Figure 1.

The microprocessor implements 39 instructions from a commercial instruction-set architecture [1]. The chip is restricted to full-word loads and stores with byte instructions emulated in software. Exceptions, system calls and stalling are all supported. Most of the control circuitry is synthesized, but a few critical sections are hand-generated. All control signals are pipelined and decoded during the cycle before they are used. The chip is fabricated in a process* that features 1µm (0.6µm effective) channel lengths, refractory gate metal (also used for intracell wiring), three levels of aluminum metallization for signal and power interconnection, and a top-level aluminum ground plane. Two-phase clocking minimizes clock skew problems. The microprocessor was designed in six months with high-level synthesis and automated physical-layout generation tools.

The 32b Ling adder, used in several sections of the chip, consists of 3598 transistors, has 2125 transistors/mm², and operates with a delay of 1.6ns. The 32b by 32word register file is similar to the on-chip instruction cache. It has 23,278 transistors with a density of 4237 transistors/mm², and is accessible in 1.7ns. Control for the chip is comprised of 14,922 transistors, with a density of 353 transistors/mm². Overall circuit density is 2474 transistors/mm².

The microprocessor and four GaAs static RAM chips make up a high-speed processing module (Figure 2). All information needed for cache miss-detection is brought on chip to minimize miss-detection delay. Instruction and data-cache tag comparators are integrated on the CPU chip. The processor communicates with an off-module MMU via a 32b bidirectional ECL-level asynchronous bus. The processor handles all cache miss processing using this bus and four 32b interface registers. The first-level memory interface can be operated in one of four modes: force-hit (buffer), force-miss, external cache (instruction and data), and internal cache (instruction).

When a cache miss or exception is detected, the address of the offending word is loaded into the instruction or data interface register, as appropriate, and the MMU is signaled that data is ready to be transmitted. The MMU reads the address over the MMU bus and returns the requested data to the appropriate register. The CPU then writes the cache tag and cache data with the updated values and releases the pipeline.

The chip interfaces to either a companion 1kx32 GaAs SRAM with GaAs I/O levels (0 to 0.7V), or to commercial ECL-I/O SRAMs. An electrically programmable pad, shown in Figure 3,

*Vitesse HGaAs III E/D MESFET process.

provides either I/O-level option. When the signal GAAS is low the pad operates as an ECL output pad. MESFET Mx is configured as a diode to provide a 0.7V drop and a 1.3V output high to conform to the ECL specification. The input stage of the GaAs RAMs are simple MESFET devices with Schottky diode gates, so the maximum voltage the pad can supply without overdriving the inputs is 0.8V. (Higher voltages may be misinterpreted.) When the GAAS signal is high, the pad output is fed back to the gate of the pullup driver. As the output turns on, negative feedback is used to reduce the driver gate voltage and clamp the output at 0.7V.

Because of high source resistance with GaAs MESFETs, only NOR gates are used. The use of only DCFL NOR gates can increase the number of gate levels on the critical paths unless special circuit structures are used. One such structure used extensively on the CPU is an Earle latch that combines a 2-input mux with a latch and a high current output buffer. This circuit is shown in Figure 4. The latch output buffer operates in a feedback mode similar to the GaAs output pad. This buffer provides a large transient current to charge the lines, then reduces its drive, providing a smaller current to maintain a stable logic high voltage.

Timing related analysis of this chip includes accurate parasitic extraction, delay calculation, back-annotation to several commercial simulation environments, delay-accurate digital simulation, critical path identification, and analysis of clock distribution. The clock analysis supports single or two-phase non-overlapping clocks. Investigation of clock skew resulted in minimization of local skew along critical paths to less than 400ps.

Portions of the chip operate at 200MHz. Full functionality is verified at 100MHz. The speed of the instruction decode in the first prototypes is limited by incorrect clock-phase assignment. Figure 5 shows outputs of the incrementor in the program counter section operating at 200MHz.

Reference

- [1] Kane, G., J. Heinrich, *MIPS RISC Architecture*, Prentice-Hall, Inc., 1992.

Transistor count	160,000
Supply voltage	2.0V
Power dissipation	24W
Signal pins	240
Power pins	236
Instructions	39
Dimensions	13.9x7.8mm ²

Table 1: Chip summary.

Figure 1: See page 268.

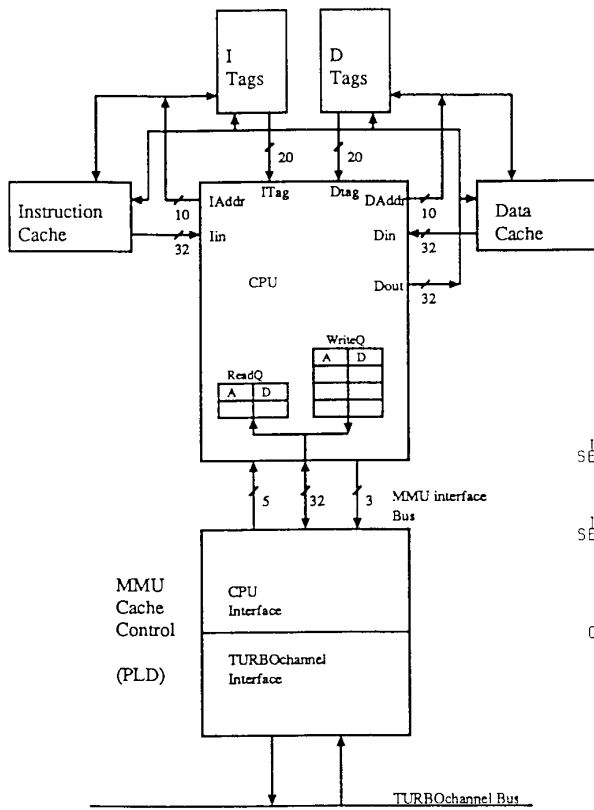


Figure 2: CPU module block diagram.

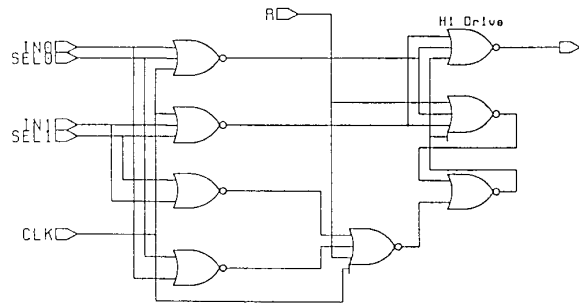


Figure 4: Mux-latch-buffer cell.

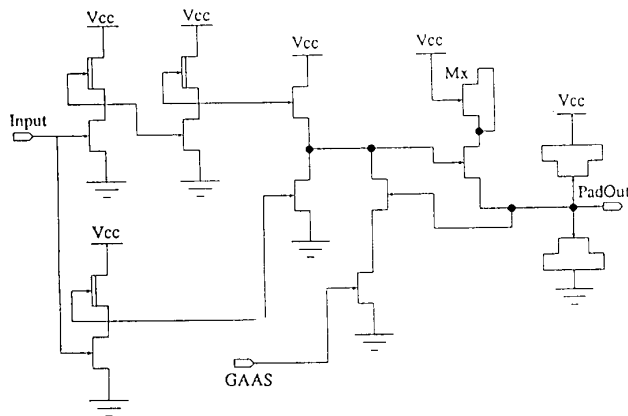


Figure 3: Electrically-programmable pad.

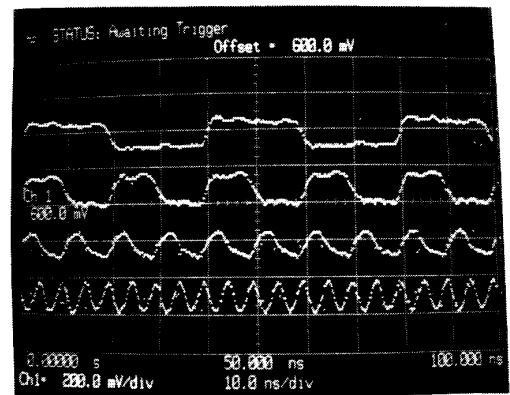


Figure 5: Program counter incrementor output waveform.

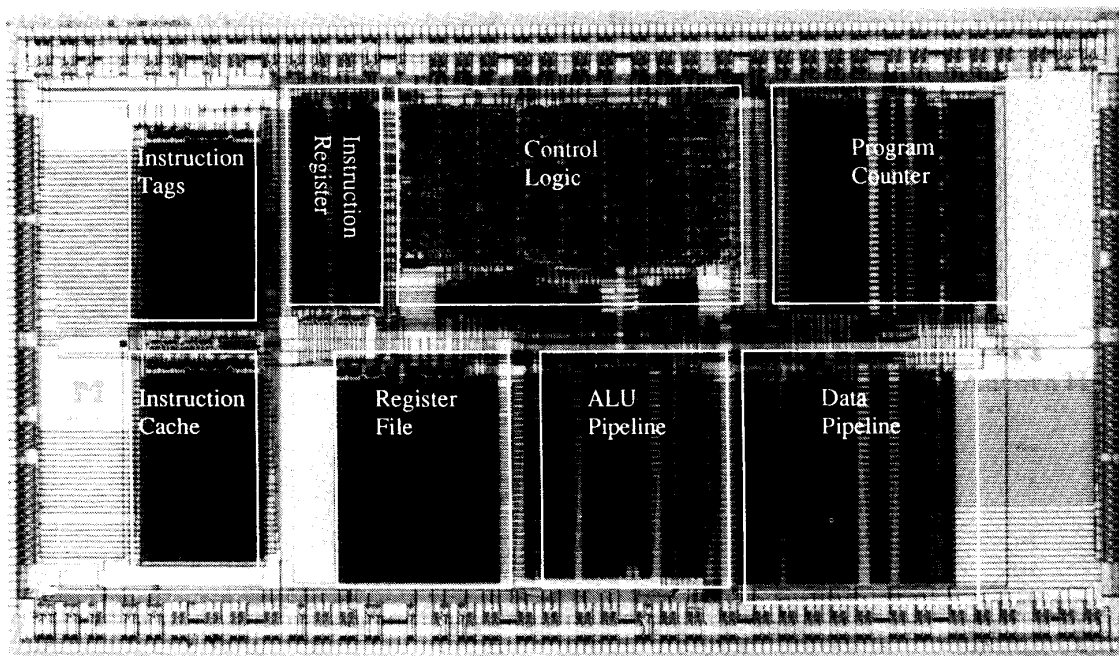


Figure 1: 160,000 Transistor GaAs microprocessor.

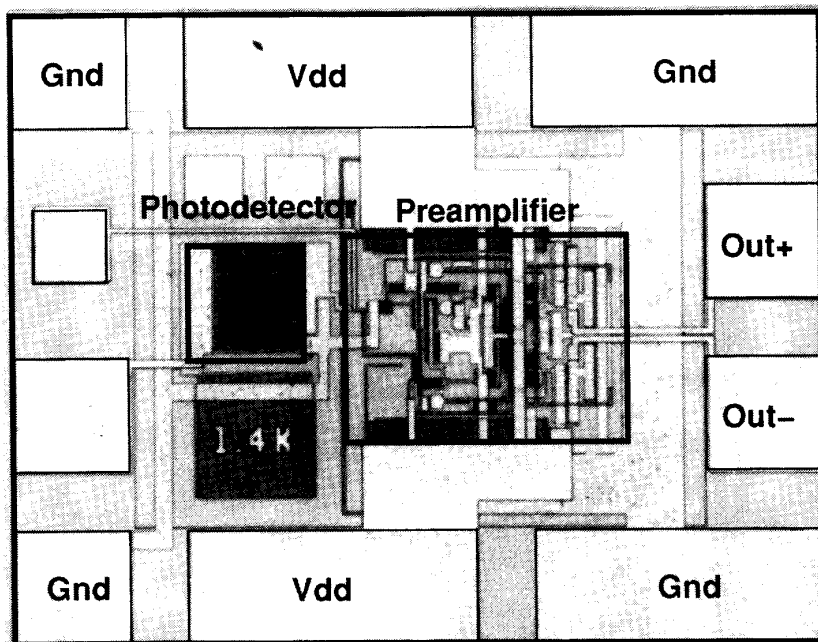


Figure 3: Chip micrograph.