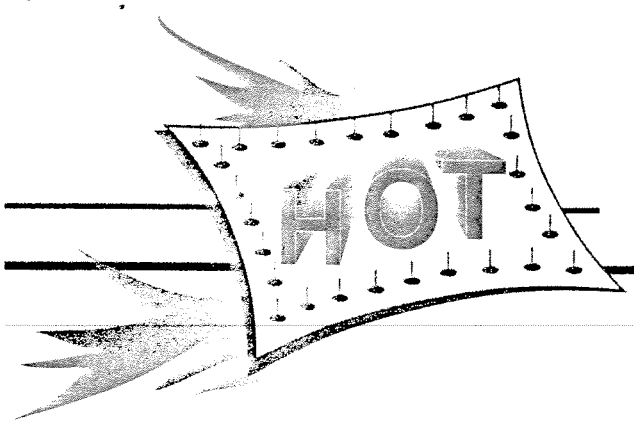
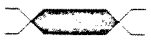


HOT Chips V

Stanford University
Stanford, California
August 8-10, 1993

Symposium Record

Sponsored by the Technical Committee on Microprocessors and Microcomputers of the IEEE Computer Society



THE AURORA PROJECT

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Advanced Computer Architecture Lab
&
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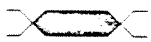
EECS Department, University of Michigan, Ann Arbor



Overview

- Technology performance metrics
- Essential process characteristics
- GaAs circuit design
- Aurora development
  - Aurora I: July 1991, 60,000 trans
  - Aurora II: July 1992, 160,000 trans
  - Aurora III: Fall 1993
    - CPU - 500,000 trans
    - FPU - 300,000 trans
    - MMU - 500,000 trans

Ring Oscillator Speed as a Performance Metric

Effect of process improvement on ring oscillator speed

	HGaAs2 Pulldown Tx = 60x1.0mm	**HGaAs3 Pulldown Tx = 60x0.6mm**	**% Change**
Fanout = 1	82.1ps	48.2	41.3
Fanout = 4	170.6	133.6	21.7
Fanout = 4 + 3mm	358.0	324.1	9.5

Process Characteristics

- Good device switching times
- High integration levels
- Good yields
- Reasonable power dissipation
- Dense, multilevel interconnect

Integration Level

- MCM delay accounts for 45% to 55% of total clock cycle
- Area utilization considers gate topology and fanin/fanout

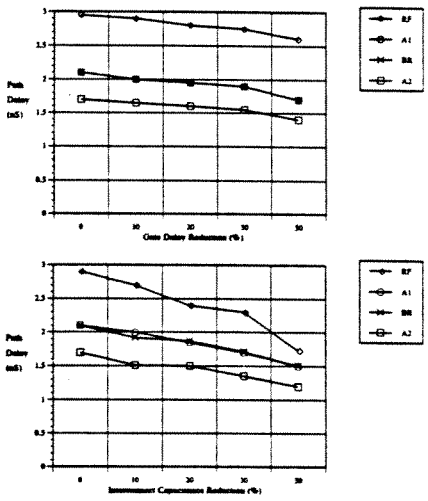
Comparison of 8x8 multipliers in three DCFL processes

	Gate Metal	Metal 1	Metal 2	Metal 3	Total Layout Area	Total Routing Area
Process A	1.00	1.00	1.00	1.00	1.00	1.00
Process B	0.90	0.60	0.50	0.28	0.49	0.21
Process C	0.50	0.97	1.11	1.43	0.97	0.82

Courtesy of Dick Oettel, Cascade Design Automation

Interconnect Technology

Effect of gate delay and interconnect loading on critical path performance

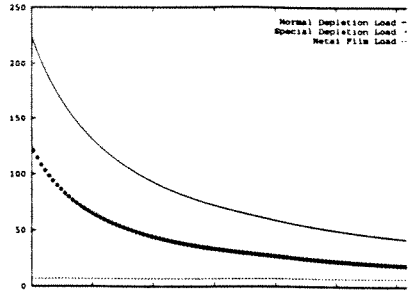


Memory Characteristics

- Dense, power-efficient caches
- Leakage currents in GaAs several orders of magnitude larger than CMOS

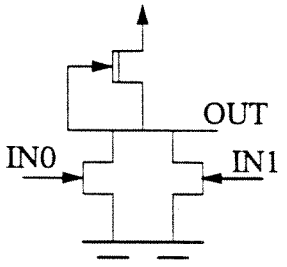
No. of Bits / Column	32	64	128	256	512
Normalized SRAM Area	1.00	0.87	0.80	0.77	0.75
Cell Area Percentage of Total Area	70.6	81.6	88.4	92.1	93.8

SRAM cell power vs cell size for 3 different load devices

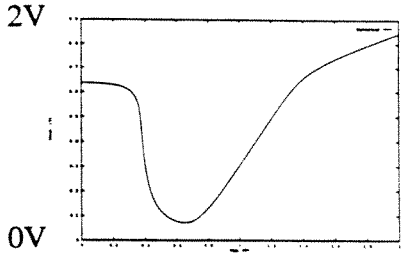


Gallium Arsenide Circuit Restrictions

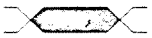
- High source resistance
- Only NOR gates
- High leakage at temperature
- Schottky diode gates limit voltage swing



2 Input GaAs NOR Gate



GaAs Inverter Transfer Function



CAD Goals

- Design time is important — automate with CAD tools
- New technologies are behind the curve without comparable CAD tools to the status quo (Si CMOS)

Our Solution

- Adapt existing Si based CAD tools to DCFL
  - Use existing commercial tools when possible
- Achieve some degree of technology independence
- Improve efficiency of all design steps
  - System level design tools
  - Synthesis from HDL descriptions
  - Verification
  - Static timing analysis
  - Datapath layout optimization

Design Flow 1

- Design specification
  - Verilog
  - Neted
- Verification
  - ◆ Verify
- Translation — GaAs Compiler
  - ◆ ChipVerilog — Verilog to Cascade netlist
  - Routexpand — Neted to Cascade netlist
- Physical design environment
  - GaAs version of Chipcrafter
- Back translation
  - Cascade to Verilog
- Physical verification
  - Dracula — DRC, LVS
- Fab and test

Aurora 1

- Single chip CPU
  - MIPS instruction set — no byte ops, MPY or DIVI
  - Full scan chain
  - 2 phase non-overlapping clock
- Test vehicle for CAD tools and testing
- Designed by 6 graduate students in about 4 months
  - 60,500 transistors
  - 12.2 mm x 7.9 mm
  - 282 signal pins (344 pin package)
  - 11 W @ 2V
- Out of fab (Vitesse through MOSIS) December 1991
- Tested Jan - Mar 1991

Design Flow 2

- System design
  - ◆ Cache-UM
- Design specification
  - – Verilog
- Verification
  - – Verify
- Translation — GaAs Compiler
  - ◆ ChipVerilog — Verilog to Cascade netlist
- Physical design environment
  - – GaAs version of Chipcrafter
  - ◆ Optimal latch placement on datapath
  - ◆ Automatic delay calculation
- Back translation
  - – Cascade to Verilog

Design Flow 2 (cont.)

- Physical verification
  - – Dracula — DRC, LVS
  - ◆ Fanout and beta ratio checking
  - ◆ Clock phase and skew checking
- Static timing analysis
  - ◆ Prototype timing analyzer (TAN)
- Fab and test

Aurora 2

- Comparison of H-GaAs II and H-GaAs III

Fanout	Propagation Delay (ps)	
	H-GaAs II	H-GaAs III
1	80	68
2	120	103
3	160	144

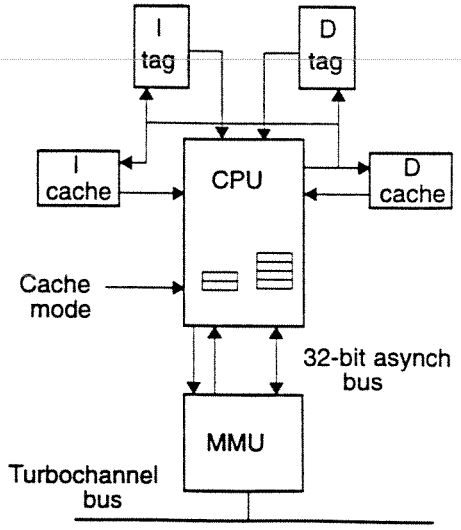
- MIPS R3000 architecture subset
  - 5 stage pipeline
  - 4 entry write buffer
  - 32 word on-chip cache
- Prototype construction
  - CPU and four 1K x 32 bit SRAM

Aurora 2 (cont.)

- Clocks
  - 2 phase non-overlapped
  - 7 stage buffer tree
  - 400 ps skew
- Circuit solutions
  - Ground plane
  - Limited fan-in
  - NOR logic
- Mux-latch-buffer cell
  - Integrates 3 common functions
  - Saves 4 levels of logic
  - 37% of total chip instance count
- I/O pads
  - GaAs/ECL programmable

Prototype System

- 32 bit asynchronous MMU bus
- 4 CPU operating modes
- 3 CPU requests
- MMU services request, supplies data
- CPU updates caches using normal pipeline
- CPU state machine handles pipeline stall and restart
- MMU built from PLDs



Critical Path

- 36 gates
  - 30% longer than next most critical path
  - No synthesized logic on critical path
- Removing critical path allows a 260 MHz clock

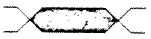
What we learned

- Large GaAs DCFL microprocessor chips are possible
- Branch architecture is critical to performance
  - More attention on minimization of path length
- More design tool support needed for 2 phase design
  - Better signal naming conventions
  - Clock phase checking program (now complete)

Density Improvement over Aurora I

- 50% due to third routing layer
- 35% through improved circuit structures
- 15% from HGaAs III process improvement

	HGaAs II Transistor Count	Density (Trans./mm^2)	HGaAs III Transistor Count	Density (Trans./mm^2)
Largest Control Block	582	1067	516	1364
Register File	21,910	2014	23,278	4253
CPU	60,500	540	160,000	1475



Design Flow 3

- System design
  - ◆ Cache-UM
  - ◆ Trace driven simulations for CPU & FPU decisions
  - ◆ In-OS simulation
  - ◆ Hardware monitoring
- Design specification
  - – Verilog
- Verification
  - ◆ Verify
- Translation to layout— "GaAs Compiler"
  - – EPOCH — Cascade Design Automation
  - ◆ Optimal latch placement on datapath
- Back translation
  - – Cascade to Verilog

Design Flow 3 (cont.)

- Functional verification
  - – Quickturn Enterprise system (180 K gate system)
- Physical verification
  - – Dracula — DRC, LVS
  - ◆ Fanout and beta ratio checking
  - ◆ Clock phase checking
- Static timing analysis
  - ◆ Prototype timing analyzer (TACTIC)
- Fab and test

Aurora 3

- Complete chip set
  - CPU — 400 MHz 500K transistors
  - FPU — 250 MHz 300K transistors
  - MMU — 500K transistors
  - SRAM — 1K x 32 for 16KB data cache
- Status
  - Verilog models execute some instructions
  - Emulation of floating point functions begun
- CPU
  - 2 execution units, instruction fetch, load/store unit
  - Reorder buffer — precise exceptions
  - High speed streaming interface
  - Decoded instruction cache (2KB)
  - Branch prediction — cut critical path by 30%
  - Performance: simulation on SPEC Int92 — CPI = 1.46
  - SPEC fp92 — CPI = 1.25, 270 and >300 with reordered code

Summary

- Computer-aided design
  - CAD tools are essential if exotic technologies are to compete with Si
  - Logic synthesis and timing tools are worth an extra instruction issue
- GaAs DCFL
  - Large DCFL chips possible
  - Power consumption compares to CMOS above 200 MHz
  - Simple process that achieves speeds only matched by advanced submicron Si