SPECIAL PURPOSE VLSI PROCESSORS FOR INDUSTRIAL ROBOTS

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1. Introduction

It is projected that by 1985 integration levels for VLSI circuits will approach one million devices [PaS80]. Even more complex systems are anticipated from the VHSIC (Very High Speed Integrated Circuits) program [Bar81]. Along with these increasing levels of integration go decreasing hardware costs. The combination of these two developments means that it is going to be cost-effective to construct special purpose computers for many of the common functions that are anticipated in industrial robotics. Indeed, this is already beginning to happen with the appearance of such products as the SRI vision module [Nit79].

The ability to realize common robotics functions as VLSI components allows the designer considerable freedom to express the function's algorithm; freedom that would not exist if the algorithm had to be implemented through several levels of software on a classical von Neumann architecture. This has several important consequences that are particularly pertinent to industrial robotics. The first of these is reliability: The system can have fault tolerance designed into it from its inception, rather than added on in hindsight. The second of these is speed to meet real-time constraints: The system can be designed to directly execute time critical sections of the target algorithm as well as take advantage of the inherent parallelism in the algorithm. This last feature is particularly relevant in the case of vision where many of the low level image processing algorithms have an extremely high degrees of inherent parallelism.

To point out what can be done in the way of developing special purpose parallel processors the next two sections outline two projects at the Unversity of Michigan to develop such processors for robot arm control and robot vision.

2. VLSI Processor for Robot Arm Control

This work has developed a preliminary specification for a VLSI implementation of a single chip parallel processor for dedicated arithmetic-intensive applications [TuM81]. Circuit densities commensurate with levels of integration projected for the mid-1980s are assumed. The proposed processor, termed the Numerical Processor (NP), is suitable for real-time control where sophisticated control strategies require very large numbers of high precision arithmetical operations to be performed for every input/output transaction. In particular, the NP is intended for the real-time control of a robot arm. The NP functions as an attached processor of a general purpose minicomputer. Conceptually, it lies between Floating Point Systems' AP-120B [Flo79], a high performance numerically oriented attached processor, and the Intel 8087 [Pal80], a single chip numerically oriented attached processor in the Intel 8087 family of components [Int79]. All three work with floating-point numbers. The NP differs from the AP120B by being much simpler, less flexible, slower, and by having a smaller word size (32 bits versus 38 bits). It differs from the 8086 by having its own on chip program memory, input/output buffers to facilitate real-time applications, and two independent pipelined function units. However, the 8087 has a more flexible number format,and can deal with several variants of the IEEE floating point standard up to and including the 80 bit format.

The preliminary study reported in [TuM81] assumed the NP will be implemented in nMOS because of our present expertise is in this technology. However, our eventual aim is to investigate the design of the NP in a faster technology that still has the density of integration associated with nMOS. A prime candidate is the I^3L (Isoplanar Integrated Injection Logic) technology developed by Fairchild. however, the n-well CMOS process presently under development in our fabrication lab is also a possibility.

As mentioned earlier, the design philosophy of the NP is oriented towards a dedicated arithmetic-intensive application, in particular, the control of a robot arm where the arm response is limited by the complexity of the control computations. The specific robot arm in mind is the Unimation PUMA 600. It is a six link arm having all revolute joints. The overall control strategy for an arm such as the PUMA involves five basic stages. These stages are as follows.

(1) A path planning stage.

(2) Orientation matrix calculation

(3) Trajectory transformation.

(4) Gross motion control.

(5) Fine Motion (Accommodation).

Stage 4 involves computing the actuator torques τ (a six vector) required to achieve the joints' angular velocities $\dot{\theta}$ and accelerations $\ddot{\theta}$ (both six vectors). This is done using an iterative set of equations [LWP80], [TML80]. Because this stage represents a potential computational bottleneck, we have simu-

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lated the Numerical Processor using these equations as a benchmark. For more on the equations see [TML80]. The results of the simulation are presented in [TuM81]. Assumptions about gates delays were based on SPICE simulations using parameters measured in our nMOS process. Based on these (conservative) figures we obtained processing rates of about 2.7 MFlops for the NP. This translates into being able to compute the values of τ every 500 μs (the values of τ need to be recomputed at every point along the trajectory, hence the need for speed). The encouraging performance figures of the simulation indicate that the NP would be a valuable component for the designer of real-time systems who is faced with compute bound bottlenecks.

3. VLSI Processor for Robot Vision

Robot vision is an area in which a considerable amount of research has been accomplished. In addition, there has been much interest in special purpose highly parallel array computers for vision computations [Ree81]. This coincides with one of our major interests which is to investigate the possibility of applying VLSI technology, in the form of special purpose computers, to improve the capability of present vision systems.

An important issue in industrial vision is that of speed. It has been estimated [ReH79] that processor bandwidths on the order of 1 to 100 billion operations per second will be required to solve some of the current problems in robot vision. While the current trend towards "massively parallel" architectures [Bat80] for vision affords a solution it raises the issue as to what algorithms can be implemented on such architectures. Our research is aimed at providing an answer to this question and further providing a candidate special purpose architecture capable of meeting the computing requirements of industrial robot vision. Our initial research has been to catalog those algorithms that a consensus of researchers considers useful, and then to consider various architectures appropriate for those algorithms. This initial work will appear in [MuD82].

4. References

[Bar81]
D. F. Barbe, "VHSIC Systems and Technology," *Computer* Vol. 14, No. 2, Feb. 1981.

[Bat80]
K. E. Batcher, "Design of a Massively Parallel Processor," *IEEE Trans. Computers*, vol. C-29, No. 9, September, 1980, pp. 836-840.

[Flo79]
Processor Handbook, Floating Point Systems, Document No. 7259-003, Feb. 1979.

[Int79]
The 8086 Family User's Manual, Intel Corp., October 1979.

[LWP80]
J. Y. S. Luh, M. W. Walker, and R.P.C. Paul, "On-Line Computational Scheme for Mechanical Manipulators," *Trans. ASME: Jour. of Dynamic Systems*, Measurement, and Control, vol. 120, June 1980, pp. 69-76.

[MuD82]
T. N. Mudge, E. J. Delp, "Special Purpose Architectures for Computer Vision," *2 Proc. 15-th Hawaii International Conference on System Sciences*, to appear.

[Nit79]
D. Nitzan, "Robotic Sensors In Programmable Automation," *2 SRI Technical Report Note 183*, March 1979.

[Pal80]
J. Palmer, "The Intel 8087 Numeric Data Processor," *Proc. 7th Annual Symp. on Computer Architecture*, La Baule, France, May 1980, pp. 174-181.

[PaS80]
D. A. Patterson, C. H. Sequin, "Design Considerations for Single-Chip Computers of the Future," *IEEE Trans. Computers*, vol. C-29, No. 2, Feb. 1980.

[Ree81]
A. P. Reeves, "Parallel Computer Architectures," *Proc. 1981 Conf. Parallel Processing*, Aug. 1981, pp. 199-206.

[ReH79]
D. R. Reddy, R. W. Hon, "Computer Architectures for Vision," in *Computer Vision and Sensor-Based Robots*, Eds. G. G. Dodd, L. Rossol, Plenum Press, New York, 1979, pp. 169-186.

[TML80]
J. L. Turney, T. N. Mudge, C.S.G. Lee, *Equivalence of Two Formulations for Robot Arm Dynamics*, SEL Report 142, ECE Department, University of Michigan, December 1980.

[TuM81]
J. L. Turney, T. N. Mudge, "VLSI Implementation of a Numerical Processor for Robotics," *Proceedings of the 27-th International Instrumentation Symposium*, Indianapolis, Indiana, April 1981, pp. 169-175. [Received a **Best Paper Award**.]