Introduction to the Special Section on Energy Efficient Computing

Trevor Mudge, *Fellow*, *IEEE*

✦

ENERGY efficient computing used to be a concern only for designers of untethered computer and mobile communication systems, where battery size and recharge intervals limited their usefulness. In the past few years, the importance of reducing energy has become a central concern for designers of tethered computers as well because of the power limitations of a standard household power outlet and because they are often deployed in large groups, in the case of server farms.

To address the research issues that arise in energy efficient computing, the US Defense Advanced Projects Agency began a program several years ago under the heading Power Aware Computing and Communications (PAC/C). This has led to a wide range of new developments in energy efficient computing and communications. This special issue solicited original papers from, but not restricted to, researchers in the PAC/C program. Our goal was to show the wide range of computer related research that is concerned with minimizing energy consumption in one way or another.

Our lead-off paper, "Genetic Approach to Minimizing Energy Consumption of VLSI Processors Using Multiple Supply Voltages," employs genetic algorithm for module selection and scheduling under the constraints of power and area.

The next paper, "Charge-Recovery Computing on Silicon," presents an overview of energy-recovering systems, focusing on recent developments.

The third paper, "A Holistic Approach to Designing Energy-Efficient Cluster Interconnects," looks at interconnecting networks of computers and addresses the problem of designing the interconnects to be energy-efficient.

The fourth paper, "Clustered Loop Buffer Organization for Low Energy VLIW Embedded Processors," focuses on the microarchitectural level and proposes and analyzes a clustered loop buffer for VLIW-style processors. The analysis shows that such buffers are able to generate a significant amount of energy savings.

The fifth paper in our series, "Power-Performance Simulation and Design Strategies for Single-Chip Heterogeneous Multiprocessors," moves to a higher level of abstraction and proposes a fast and efficient approach for designing and estimating energy consumption for single chip heterogeneous multiprocessors—a common platform for mobile system.

The sixth paper, "An Energy Efficient Instruction Set Synthesis Framework for Low Power Embedded System Designs," returns to the microarchitectural level. It proposes a design time instruction set minimization to reduce instruction cache power.

The seventh paper, "Power and Performance Analysis of Motion Estimation Based on Hardware and Software Realizations," looks at the application level, specifically the power-performance of motion detection in an image processing application.

The eighth paper, "Design Considerations for Ultra-Low Energy Wireless Microsensor Nodes," is a tutorial paper on sensor networks with special emphasis on their power requirements.

The penultimate paper, "A Speculative Control Scheme for an Energy-Efficient Banked Register File," again returns to the microarchitectural level and shows how low power register files can be constructed from smaller faster banks of registers.

The last paper, "GAARP: A Power-Aware GALS Architecture for Real-Time Algorithm-Specific Tasks," proposes an adaptive scalable architecture targeted toward algorithm-specific tasks in which power is a constraint. The architectural model derives its scalability from a set of Globally Asynchronous and Locally Synchronous (GALS) building blocks.

Trevor Mudge
Guest Editor

Trevor Mudge received the PhD degree in computer science from the University of Illinois. Since then, he has been at the University of Michigan. He was named the Bredt Professor of Engineering after a 10-year term as director of the Advanced Computer Architecture Laboratory —a group of a dozen faculty and 80 graduate students. He is the author of numerous papers on computer architecture, programming languages, VLSI design, and computer vision. He has also chaired 32 theses in these research areas. He is a fellow of the IEEE and a member of the ACM, the IEE, and the British Computer Society.

● *The author is with the Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, MI 48109-2122. E-mail: tnm@eecs.umich.edu.*